IN THE CLAIMS:

Please cancel claims 1, 3 and 18 without prejudice, and amend the claims as follows:

1. – 3. (Canceled)

4. (Currently Amended) A method for refreshing dynamic memory cells arranged along word lines and bit lines, comprising:

generating a refresh signal to activate a word line to refresh a charge stored in memory cells arranged on the word line;

monitoring an amount of charge loss of one or more sets of dynamic reference cells; and

adjusting a frequency of the refresh signal based on the monitored amount of charge loss, wherein the frequency of the refresh signal is adjusted by dividing a fundamental frequency by a frequency divider value, wherein adjusting the frequency of the refresh signal comprises adjusting the frequency divider value, and ~~The method of claim 3,~~ wherein adjusting the frequency divider value comprises:

increasing the frequency divider value if the monitored amount of charge loss falls below a first threshold value; and

decreasing the frequency divider value if the monitored amount of charge loss exceeds a second threshold value.

5. (Original) The method of claim 4, wherein the first and second threshold values are different.

6. (Currently Amended) The method of claim 4 ~~claim 1~~, wherein monitoring the amount of charge loss of the one or more sets of reference cells comprises:

precharging a first set of the reference cells on a first reference word line to a first potential value;

isolating the first set of reference cells from a first common bit line;

a known time later, connecting the first set of reference cells to the first common bit line; and

comparing a potential on the first common bit line with a first reference potential.

7. (Original) The method of claim 6, further comprising precharging the first common bit line to a center potential.

8. (Original) The method of claim 6, wherein the first reference potential is a ground reference.

9. (Original) The method of claim 6, further comprising:

precharging a second set of the reference cells on a second reference word line to a second potential value;

isolating the second set of reference cells from a second common bit line;

a known time later, connecting the second set of reference cells to the second common bit line; and

comparing a potential on the second common bit line with a second reference potential.

10. (Original) The method of claim 9, wherein adjusting the frequency of the refresh signal based on the monitored amount of charge loss comprises:

increasing the frequency of the refresh signal if the potential on the first common bit line exceeds the first reference potential or the second reference potential exceeds the potential on the second common bit line; and

decreasing the frequency of the refresh signal if the first reference potential exceeds the potential on the first common bit line and the potential on the second common bit line exceeds the second reference potential.

11. (Currently Amended) A circuit for adjusting a frequency of a refresh signal used to refresh dynamic memory cells, comprising:

a first set of reference cells connectable to a first common bit line by activation of a first common word line;

a second set of reference cells connectable to a second common bit line by activation of a second common word line; and

a regulating unit comprising a frequency divider circuit and a counter for storing a frequency divider value for controlling the frequency divider circuit, the regulating unit configured to monitor an amount of charge loss of the first and second reference cells and adjust the frequency of the refresh signal used to refresh the dynamic memory cells based on the monitored amount of charge loss, wherein the frequency of the refresh signal is adjusted by dividing a fundamental frequency by [[a]] the frequency divider value.

12. (Original) The circuit of claim 11, wherein the regulating unit is configured to generate one or more control signals to activate the first and second sets of reference cells in order to monitor the amount of charge loss of the first and second reference cells.

13. (Original) The circuit of claim 11, wherein the regulating unit is configured to:

increase the frequency of the refresh signal if the loss of charge of either the first and second sets of reference cells exceeds a threshold amount; and

decrease the frequency of the refresh signal if the loss of charge of both the first and second sets of reference cells does not exceed the threshold amount.

14. (Currently Amended) The circuit of claim 11, wherein the regulating circuit is configured to:

precharge the first and second sets of reference cells to respective first and second potential values;

~~isolating~~ isolate the first and sets of reference cells from the respective first and second common bit lines;

a known time later, connect the first and second sets of reference cells to the respective first and second common bit lines;

determine the charge loss of the first set of reference cells by comparing a potential on the first common bit line with a first reference potential; and

determine the charge loss of the second set of reference cells by comparing a potential on the second common bit line with a second reference potential.

15. (Original) The circuit of claim 14, wherein:

the first potential value is ground;

the second potential value is above ground;

the regulating unit is configured to increase the frequency of the refresh signal if the potential on the first common bit line exceeds the first reference potential, the second reference potential exceeds the potential on the second common bit line, or both; and

the regulating unit is configured to decrease the frequency of the refresh signal if the first reference potential exceeds the potential on the first common bit line and the potential on the second common bit line exceeds the second reference potential.

16. (Original) The circuit of claim 14, wherein the regulating circuit is configured to precharge the first and second common bit lines to a center potential prior to connecting the first and second sets of reference cells to the respective first and second common bit lines.

17. (Original) The circuit of claim 11, wherein the regulating unit initiates the monitoring of charge loss of the first and second sets of reference cells and the adjusting of the frequency of the refresh signal based on one or more word address signals received from a refresh circuit.

18. (Canceled)

19. (Currently Amended) A memory device, comprising:

a plurality of dynamic memory cells arranged along word lines and bit lines of the device;

at least a first set of reference cells arranged around a first common word line and a first common bit line;

a refresh circuit for generating a refresh signal to refresh the dynamic memory cells; and

a refresh frequency adjust circuit to adjust a frequency of the refresh signal based on a monitored amount of charge loss of the first set of reference cells, wherein the frequency of the refresh signal is adjusted by dividing a fundamental frequency by a frequency divider value.

~~The memory device of claim 18,~~ wherein:

the frequency of the refresh signal is established by dividing the fundamental frequency of an oscillator circuit by a counter value, the counter value being the frequency divider value; and

the refresh frequency adjust circuit is configured to adjust the frequency of the refresh signal by adjusting the counter value.

20. (Currently Amended) The memory device of claim 19 ~~claim 18~~, further comprising:

at least a second set of reference cells arranged around a second common word line and a second common bit line; and

wherein the refresh frequency adjust circuit is configured to adjust the frequency of the refresh signal based on a monitored amount of charge loss of both the first and second sets of reference cells.

21. (Currently Amended) A circuit for adjusting a frequency of a refresh signal used to refresh dynamic memory cells, comprising:

a first set of reference cells connectable to a first common bit line by activation of a first common word line;

an oscillator configured to output a clock signal at a fundamental frequency;

a regulating circuit configured to:

monitor an amount of charge loss of the first reference cells; and

set a divider value on the basis of the amount of charge loss;

a frequency divider circuit configured to divide the clock signal at the fundamental frequency by the divider value, thereby producing the refresh signal at an adjusted frequency; and

a counter configured to store the divider value.

Please add the following new claims:

22. (New) The circuit of claim 21, wherein the regulator circuit is further configured to:

increase the divider value if the monitored amount of charge loss falls below a first threshold value; and

decrease the divider value if the monitored amount of charge loss exceeds a second threshold value.

23. (New) The circuit of claim 22, further comprising:

a second set of reference cells arranged around a second common word line and a second common bit line; and

wherein the regulating circuit is further configured to adjust the divider value based on a monitored amount of charge loss of both the first and second sets of reference cells.

24. (New) The circuit of claim 23, wherein the regulating circuit is further configured to:

precharge the first and second sets of reference cells to respective first and second potential values;

isolate the first and sets of reference cells from the respective first and second common bit lines;

connect, after a predetermined delay time, the first and second sets of reference cells to the respective first and second common bit lines;

determine the charge loss of the first set of reference cells by comparing a potential on the first common bit line with a first reference potential; and

determine the charge loss of the second set of reference cells by comparing a potential on the second common bit line with a second reference potential.